

REMARKS/ARGUMENTS

Please enter the amendment under the provisions of 37 CFR 1.1126. It is respectfully submitted that the amendment to claim 1 has not changed the substance of claim 1 as originally filed or as previously amended. The examiner objected to the use of the term "otherwise". The applicant attempted to remove that objection with the previous amendment. The applicant now again tries to remove that objection. However, the claim is the same in substance as originally filed and this amendment does not raise any new issues. Therefore, this amendment should be entered for purposes of appeal.

Further, the substantive issue still remains, and that is whether Lentz et al. grants default access to the bus to a predetermined one of the candidates. More particularly, the essential issue here is whether, in the default case when no candidate is requesting the bus, the action of "**assigning** a priority", as in Lentz et al., is a different action than actually "**granting** access to the bus", as claimed.

In the art, the action of granting bus access to a given candidate in the absence of a bus request by *any* of the candidates is referred to as "parking" the given candidate on the bus. The significant difference between "parked" and "non-parked" arbitration schemes is well known in the art and is described, by example, in the attached pages 9-13 and 9-14 of the MPC7450 RISC Microprocessor Family User's Manual by Motorola.

Thus, as pointed out in the applicant's previous response, the claim states that one of the candidates *is granted* access to the bus, *even in the absence of any bus request (the "default")*. Thus, even assuming arguendo that Lentz et al. *assigns* a highest priority to a candidate in the absence of any bus request, as alleged by the examiner, the applicant takes the process *one step further* by actually granting access to the bus to the predetermined one

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of the candidates. The examiner has not pointed out where Lentz et al. describes this further granting step. The applicant again requests that the examiner point out the column and line number where Lentz et al. allegedly states that the highest priory candidate is *actually granted access to the bus in the absence of a bus request*.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

Date

1-8-04



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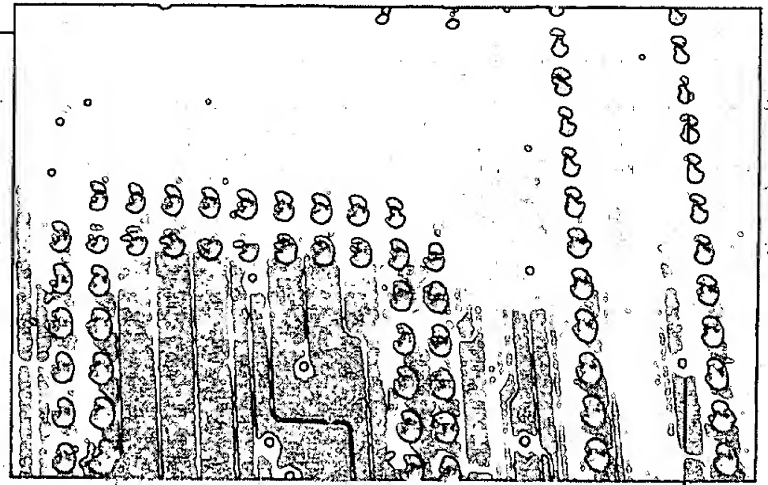
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**MPC7450 RISC Microprocessor
Family User's Manual**

Devices Supported:

**MPC7455, MPC7451, MPC7450,
MPC7445, MPC7441**

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the first tenure is asserted, grant in order to optimize

critical timing paths in the Removal of ABB does, the arbiter that must track it (BG) to a processor when a tenure from another bus

master can be granted the exclusive). In single-master using the bus to the only (g). However, as explained s AACK

if it receives the qualified re accepting a qualified bus due to a HIT and there is next

ot parked (BG is negated), holds it asserted until ified MPX bus grant is as

red state variables) is not asserted in the er the master or any other on-parked case; the X's grant. Note that ABB (as neither is address is available.

flow

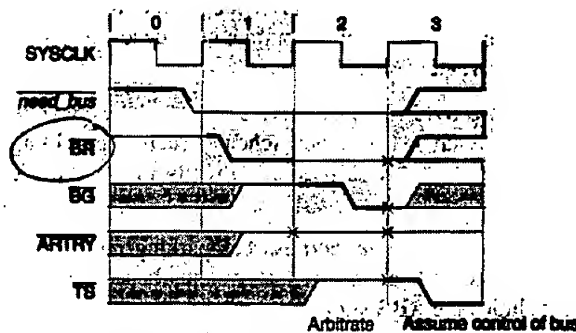


Figure 9-4. MPX Address Bus Arbitration—Non-Parked Case

9.3.1.2 MPX Address Bus Parking

External arbiters must allow only one device at a time to be the address bus master. In systems with only a single master, BG can be grounded (always asserted) to continually grant mastership of the address bus to the MPC7451. This continual granting of mastership is called bus parking.

If the MPC7451 asserts BR before the external arbiter asserts BG, the MPC7451 is considered unparked, as shown in Figure 9-4. Figure 9-5 shows the parked case, where a qualified bus grant exists on the clock edge following a need_bus condition.

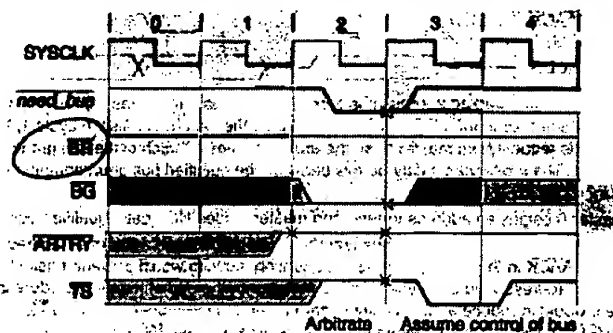


Figure 9-5. MPX Address Bus Arbitration—Parked Case

Whereas a non-parked processor must continually reassert BR to the arbiter in order to receive a bus grant, bus parking allows the arbiter to hold BG asserted. Parking permits the processor to skip the bus request (note its inactivity in Figure 9-5) and on the next cycle assume address bus ownership. Address bus tenures can be driven every other cycle by the same master.

MPX Bus Address Tenure

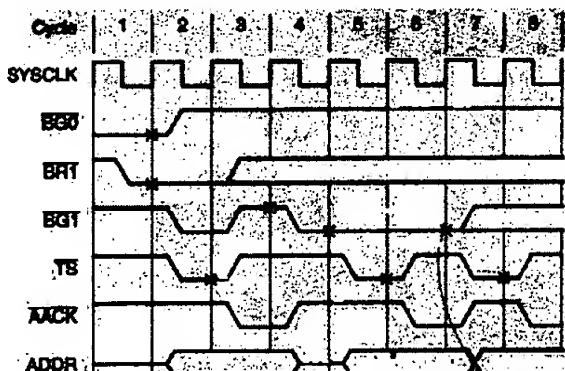
BENEFIT
OF
PARKING

The overall access latency for the memory transaction is shortened by one cycle: the system gains back not only the arbitration latency, but also the dead cycle that is between each tenure in the MPX bus interface.

Typically, bus parking is provided to the device that was the most recent bus master; however, system designers may choose other schemes such as providing unrequested bus grants in situations where it is easy to predict correctly the next device requesting bus mastership.

From the system arbiter's perspective, address bus parking must be implemented more carefully in MPX bus systems than in 60x bus systems because the qualified bus grant equation no longer includes the \overline{ABB} signal.

As shown in Figure 9-6, optimal address parking can be implemented in a multimaster system because \overline{TS} is still in the qualified bus grant equation for MPX bus masters.



Cycle 1: Master 0 has a parked address bus grant. Master 0 has an address tenure ready and a qualified bus grant, so it queues an address tenure for the next cycle. Also in cycle 1, the arbiter samples a bus request from master 1, so the arbiter queues a switch of the bus grants from master 0 to master 1. The arbiter can safely do this because the qualified bus grant equation for MPX bus masters includes \overline{TS} .

Cycle 2: Master 0 begins an address tenure, and master 1 does NOT get a qualified bus grant.

Cycle 3: The arbiter MUST negate the bus grant to master 1 because, without an address bus busy indication or \overline{AACK} in the qualified bus grant equation, nothing would prevent master 1 from beginning an address tenure in cycle 4 and colliding with the end of master 0's address tenure. Because it would introduce a difficult timing path to require the arbiter to sample \overline{TS} in cycle 2 and negate \overline{BGT} in cycle 3, it is suggested that arbiters always pulse \overline{BGR} high a cycle after swapping \overline{BGR} and \overline{BGT} , only reasserting \overline{BGR} after \overline{AACK} has been driven.

Cycle 4: The arbiter reasserts \overline{BGT} because it asserted \overline{AACK} in the previous cycle. (If the arbiter does not know in advance when \overline{AACK} is to be asserted, this timing might be difficult, and the reassertion of bus grant may have to be delayed a cycle, but most systems should be able to do this.)

Cycle 5: Master 1 gets to start its address tenure. Note that this is the optimal timing for a new master to drive the address bus.

Cycles 6 and 7: The arbiter speculatively parks \overline{BGT} enabling master 1 to begin another address tenure immediately in cycle 7.

Figure 9-6. Address Parking in MPX Bus Multiprocessor Systems

9.3.2 MPX Bus A

During the address transfer

Snooping logic may monitor bus snooping in Section 9. In this phase are transfer state tables.

The MPC7451 supports : operated on (or munged) b is performed internally bei little-endian mode is sele That is, byte address 0 of the most significant (left-n swapping or other operati MPC7451 is interfaced to

Note that the MPC7451 c mode if misaligned data is

The signals used in the ad

- Address transfer st
- Address transfer si
- Address transfer at (TSIZ[0:2]), transf global (GBL)

The MPC7451 can be HID0[XAEN]. When exte output, the four most sig cannot be left floating. If by the system during the a pulldown resistor. When e a 36 bit physical address.

Figure 9-7 shows that the address transfer and add grouping in Figure 9-7. I transfer and the address synchronous bus).

In Figure 9-7, the address in bus clock cycle 0, and the address bus terminati